

**REV: 1.4**

**SHEET**

**TITLE**

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU LGA1156-A
05	CPU LGA1156-B
06	CPU LGA1156-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	DDR III POWER CAP
10	PCH_FDI,DMI,USB,PCIE,NVRAM
11	PCH_DP,CLK BUFFER
12	PCH_HOST,SATA,PCI
13	PCH_GPIO,CTRL,AUDIO
14	PCH_PWR,GND
15	PCI_EXPRESS*16 SLOT
16	PCI_EXPRESS*4 SLOT
17	PCI SLOT 1,2
18	ITE 8720 LPC IO
19	Dual BIOS,PHOT,D-OC
20	ALC888B-VD2
21	REAR AUDIO JACK
22	CLOCK GEN ICS9LPRS914
23	DISCRETE POWER
24	DDR 15V,PWR_SEQ
25	CPU_VAXG_PWM_ISL6314CRZ
26	CPU_VTT_PWM_ISL6322G
27	VCORE_PWM_ISL6334CR

**SHEET**

**TITLE**

[illegible]

GA-H55M-D2H      Version: 1.4

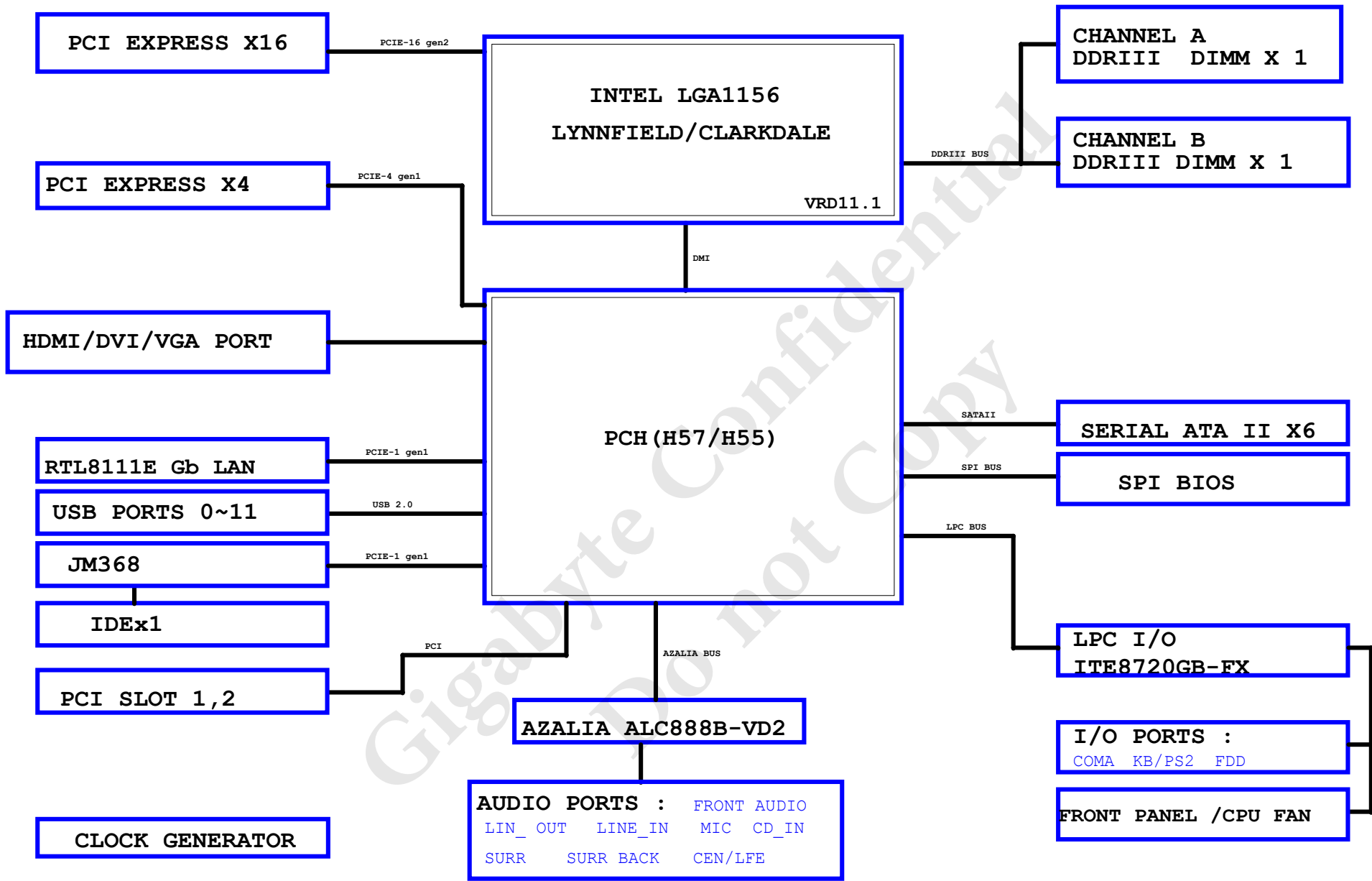
Circuit or PCB layout change  
for next version

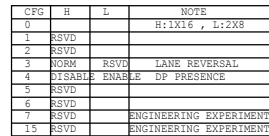
## Component value change history

2010/07/09

[illegible][illegible]

BLOCK DIAGRAM

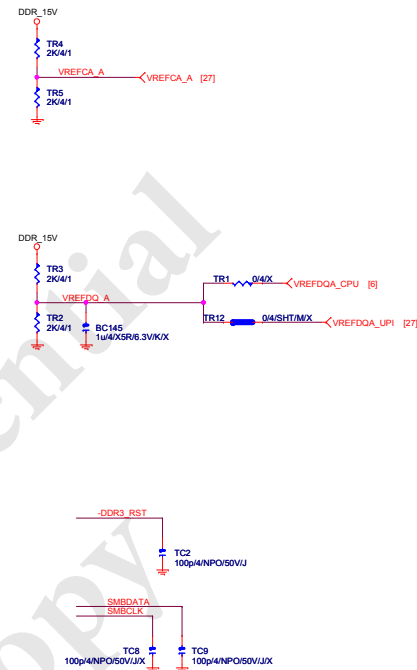
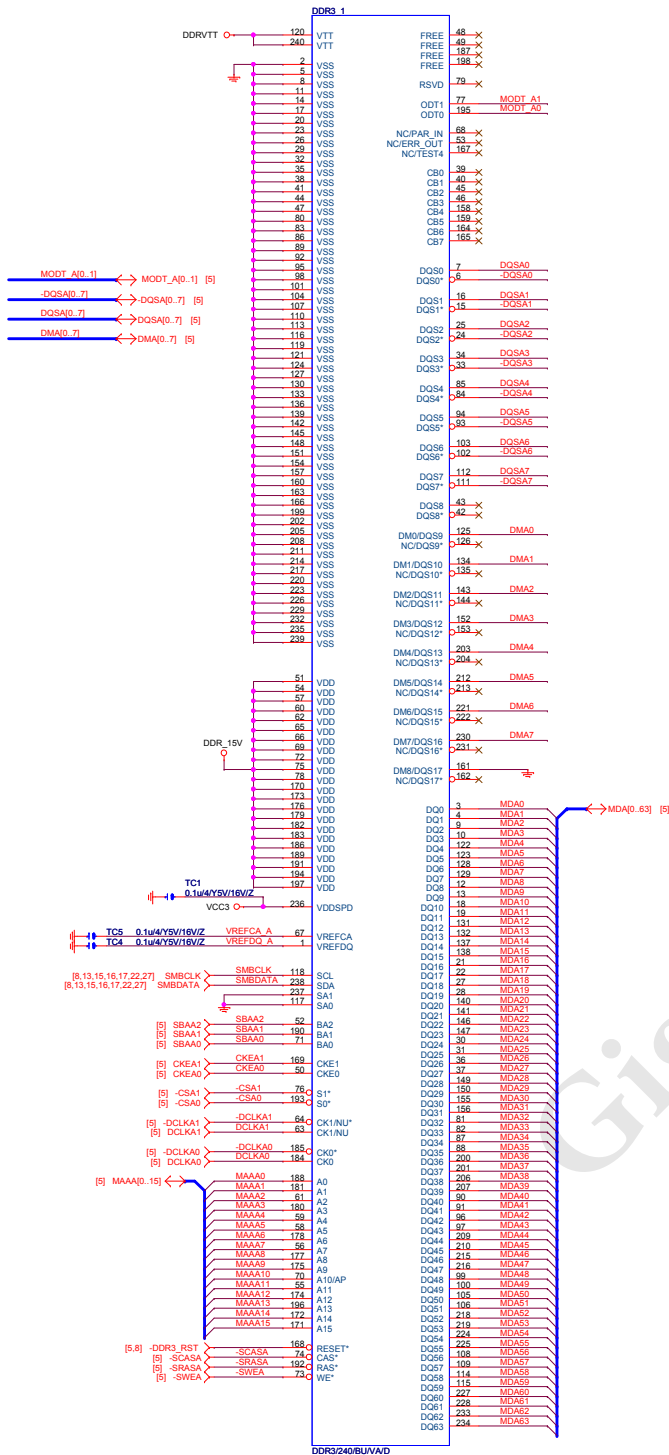




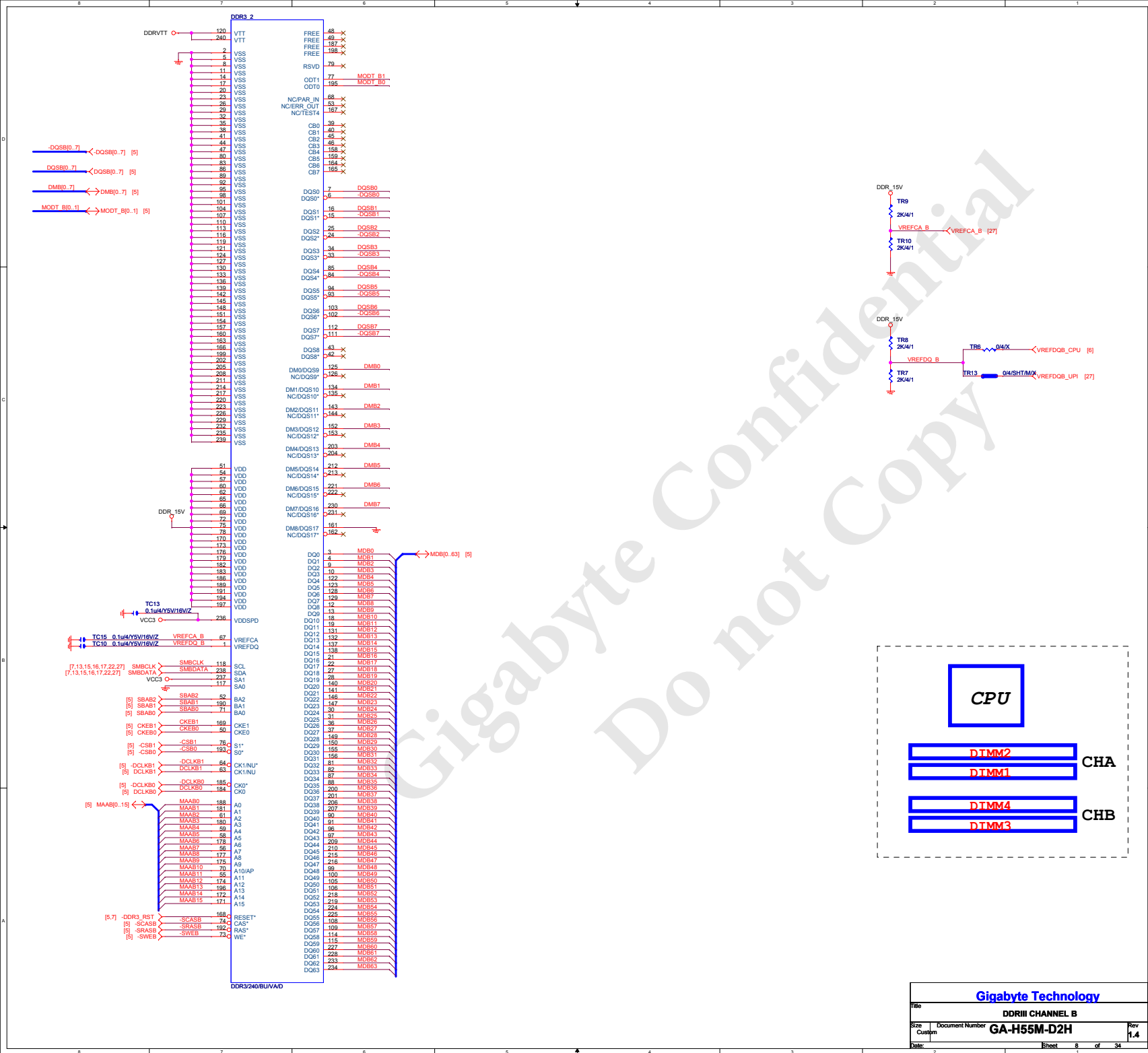
## Gigabyte Technology

LGA1156A			
MAAA0	AW18	SA_MA[0]	AK3 DQSA0
MAAA1	AY15	SA_MA[1]	AK3 -DQSA0
MAAA2	AW15	SA_MA[2]	AK2 DMA0
MAAA3	AU15	SA_MA[3]	
MAAA4	AW14	SA_MA[4]	AH1 MDA0
MAAA5	AY13	SA_MA[5]	AJ4 MDA1
MAAA6	AV14	SA_MA[6]	AL2 MDA2
MAAA7	AW13	SA_MA[7]	AL1 MDA3
MAAA8	AU14	SA_MA[8]	AG2 MDA4
MAAA9	AW12	SA_MA[9]	AH2 MDA5
MAAA10	AT19	SA_MA[10]	AK1 MDA6
MAAA11	AU11	SA_MA[11]	AK2 MDA7
MAAA12	AW11	SA_MA[12]	
MAAA13	AU24	SA_MA[13]	AP2 DQSA1
MAAA14	AT11	SA_MA[14]	AP3 -DQSA1
MAAA15	AR10	SA_MA[15]	AN1 DMA1
[7] -SWEA	AT22	SA_WE#	AN3 MDA8
[7] -SCASA	AU22	SA_CAS#	AN2 MDA9
[7] -SRASA	AT20	SA_RAS#	AR3 MDA10
[7] SBAA0	AV20	SA_BS[0]	AR2 MDA11
[7] SBAA1	AU19	SA_BS[1]	AM3 MDA12
[7] SBAA2	AU12	SA_BS[2]	AM2 MDA13
		SA_BS[3]	AP1 MDA14
		SA_BS[4]	AR4 MDA15
		SA_BS[5]	
[7] -CSA0	AV21	SA_CS#0	AL4 DQSA2
[7] -CSA1	AW24	SA_CS#1	AL3 -DQSA2
	AY23	SA_CS#2	AU1 DMA2
		SA_CS#3	
[7] CKEA0	AU10	SA_CKE[0]	AT4 MDA16
[7] CKEA1	AW10	SA_CKE[1]	AU2 MDA17
	AV10	SA_CKE[2]	AW3 MDA18
	AY10	SA_CKE[3]	AW4 MDA19
		SA_CKE[4]	AT3 MDA20
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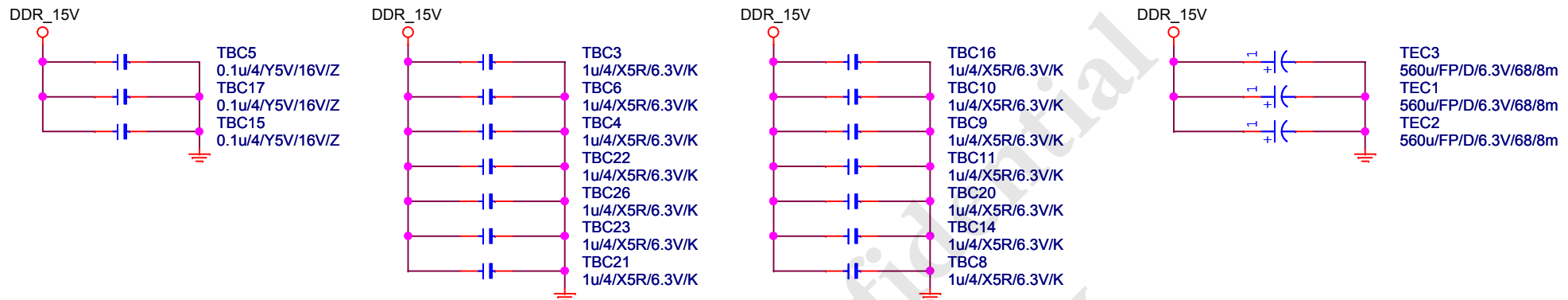




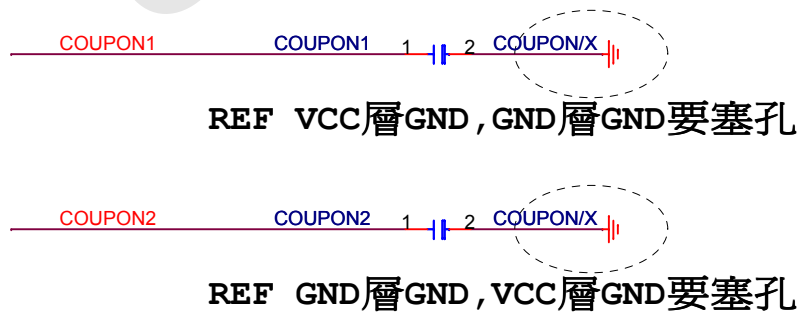
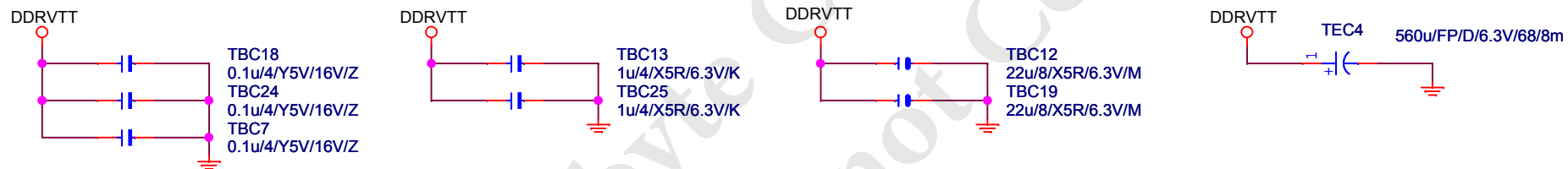


# DDR TERMINATION CHANNEL A/B

## DDR15V Decouple



## DDRVTT Decouple



**Gigabyte Technology**

Title			DDRIII POWER CAP
Size A	Document Number	GA-H55M-D2H	
Date: Thursday, July 01, 2010		Sheet 9 of 34	Rev 1.4

DMI:12/5/5/5/12  
Impedance=80 +- 17.5%

USB:15/4.5/7.5/4.5/15  
Impedance=90+- 15%

Impedance=80 +- 17.5%  
PCIE X1 :15/5/5/5/15

PCIE X4

JMB368

LAN

电容要靠近 slot 端

PCH\_HS

PCH\_HS[12SP2-030030-C1R\_12SP2-030030-C2R]

PCBH

BD82H55/BGA951

USB

PCI-E

2 OF 11

H55-->PORT6,7:N/A

OC[3:0]# for  
Device 29  
(ports 0-7)  
OC[7:4]# for  
Device 26  
(ports 8-13)

USB OC# Configure	
OC0#	USB0,1 (F_USB1)
OC1#	USB2,3 (F_USB2)
OC2#	USB4,5 (USB_LAN)
OC3#	USB6,7 (X) H55-->N/A
OC4#	USB8,9 (R_USB)
OC5#	USB10~11 (R_USB)
OC6#	USB12~13 (KB_USB)
OC7#	GPIO14

NV ALE	
Hi	Enable Danbury
Lo	Disable Danbury

Intel anti theft techonlogy

PCHE

NVRAM

BD82H55/BGA951

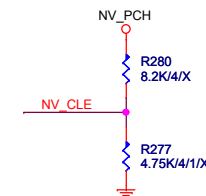
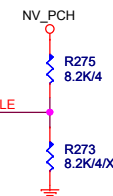
Impedance=50+- 15%

ONFI: NV\_DQ 4/5

NV\_DQS 4/10

NV\_CTRL 4/10

NV\_CK 4/15

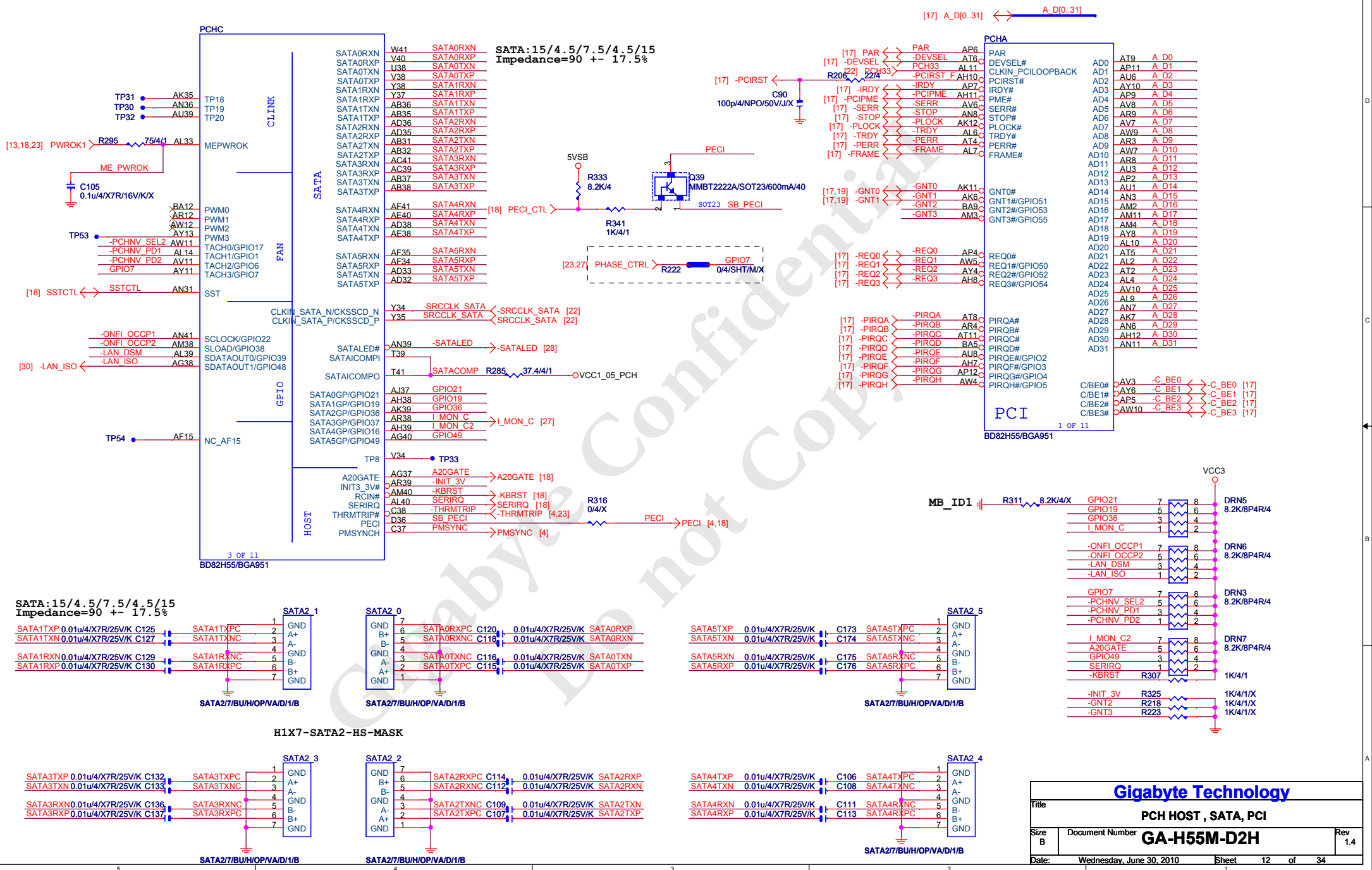


DMI Terminator voltage  
HI : AC COUP : TX/RX TO VCC  
LO : DC COUP : HALF SWING

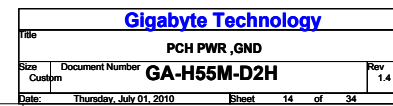
Gigabyte Technology

Title		
PCH FDI,DMI,USB,PCIE,NVRAM		
Size B	Document Number	Rev 1.4
GA-H55M-D2H		
Date:	Thursday, July 01, 2010	Sheet 10 of 34

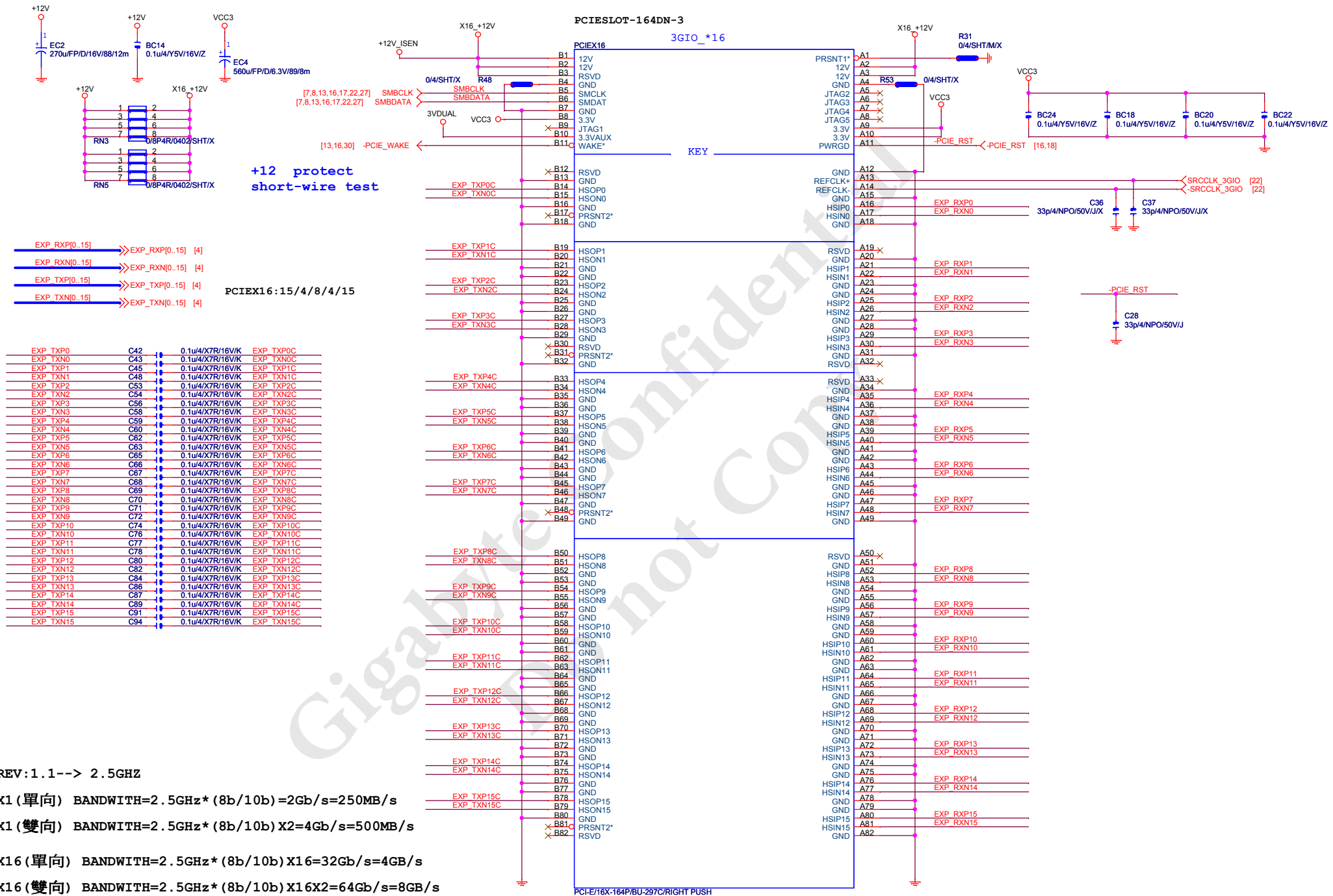








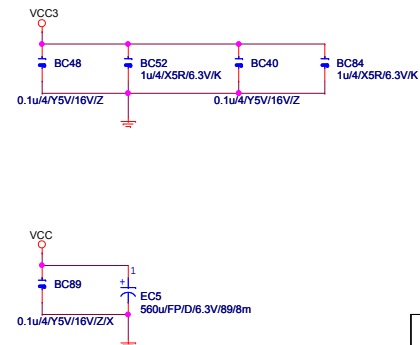
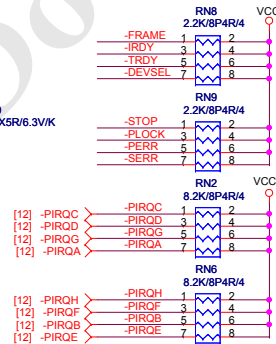
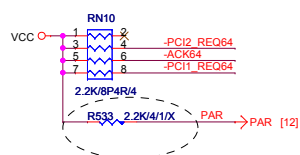
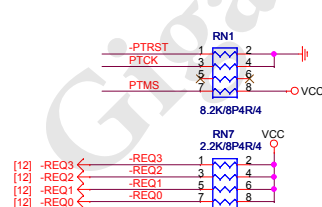
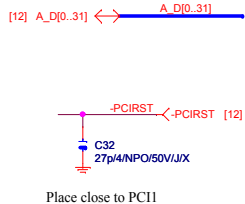
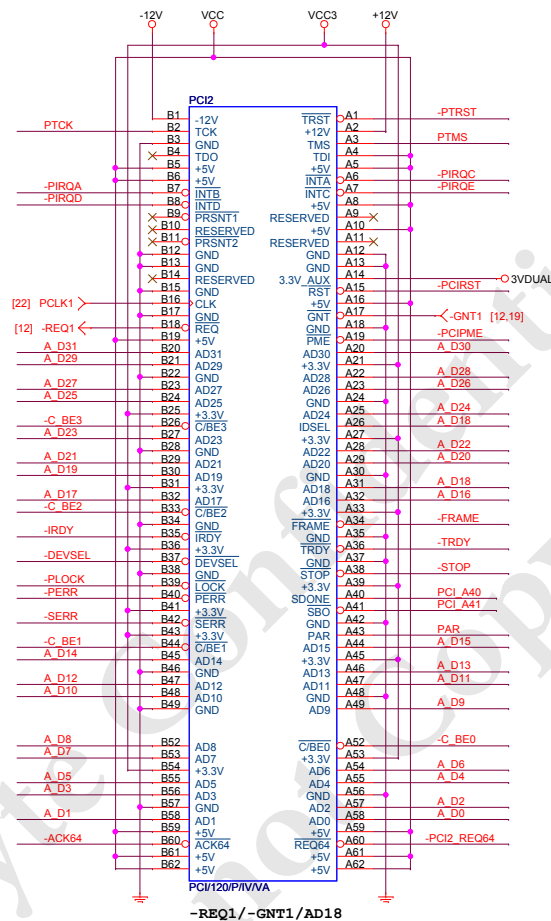
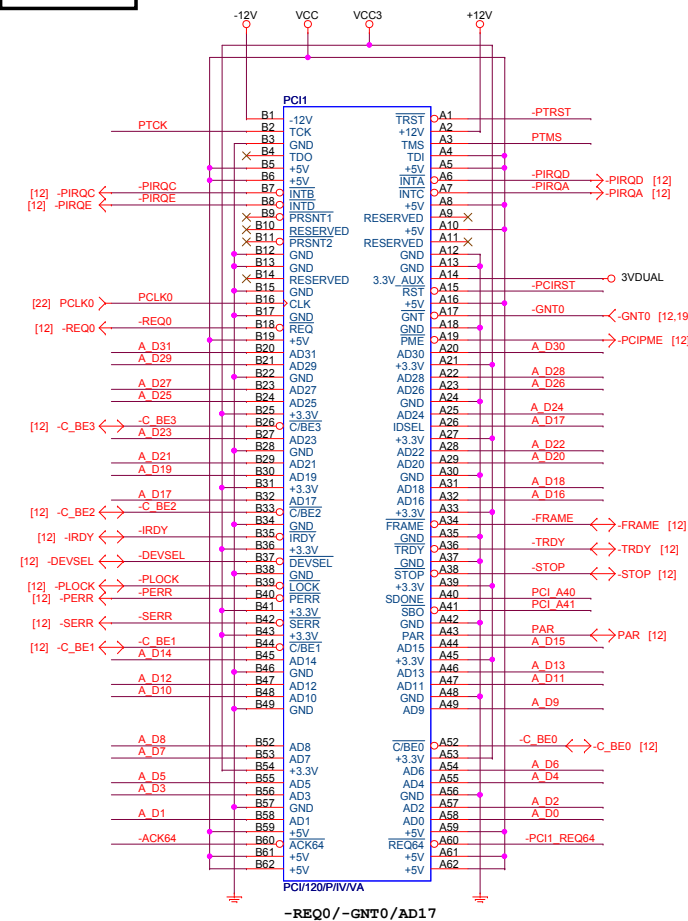








PCI1,2 SLOT
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# IT8720F ( GB )

IT8720F-S-JX/GBYS

For IT8721 to control PCH PECI

For IT8720 Power

For IT8721 Power

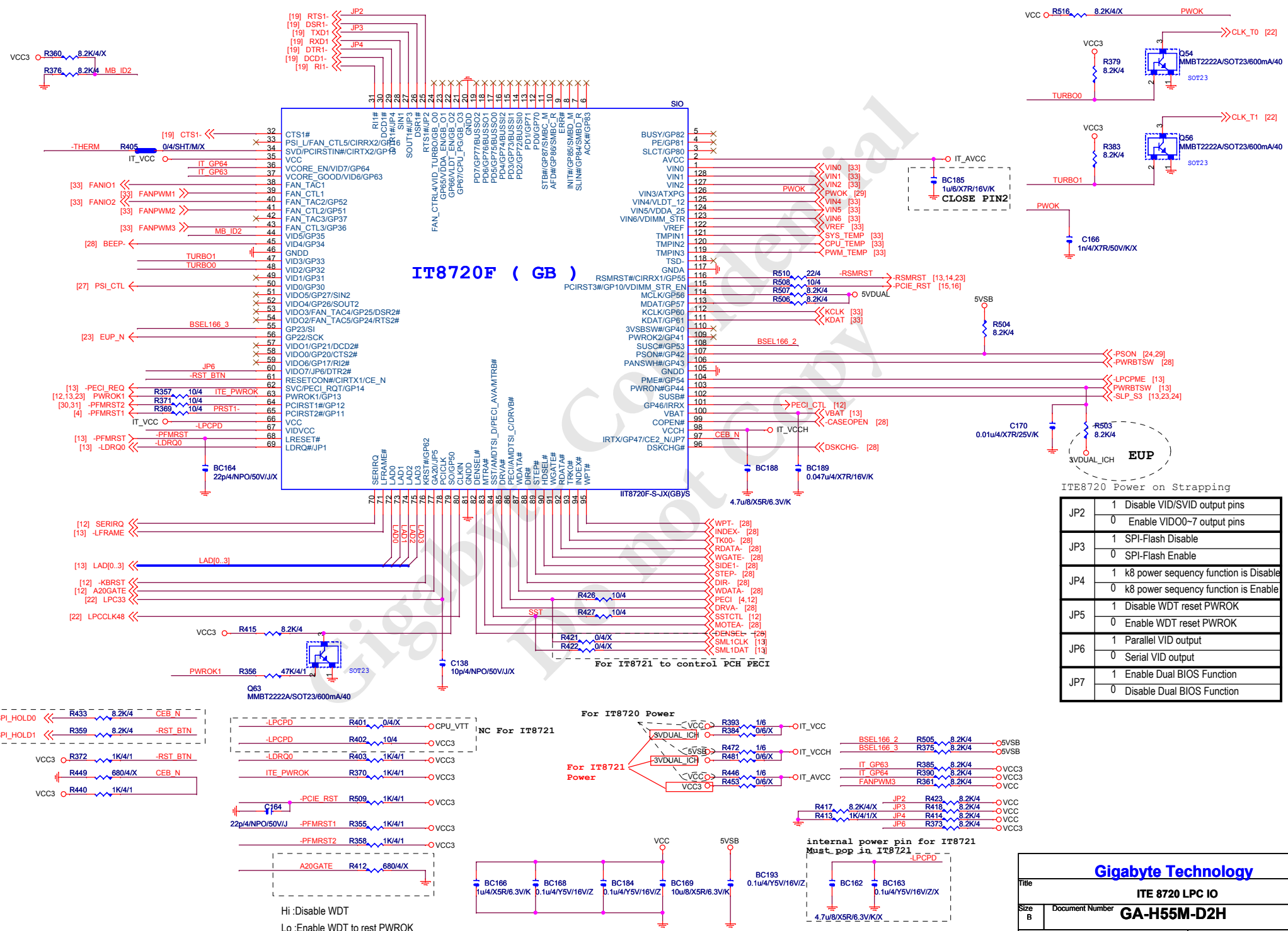
internal power pin for IT8721  
Must pop in IT8721

ITE8720 Power on Strapping

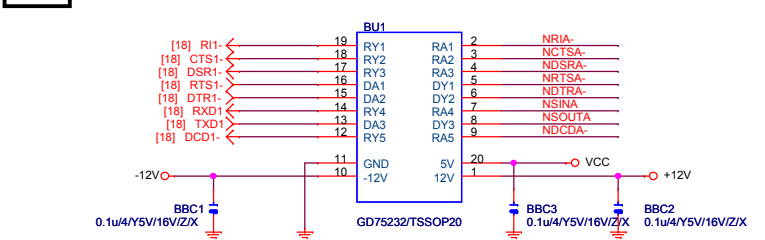
JP2	1	Disable VID/SVID output pins
JP2	0	Enable VID00-7 output pins
JP3	1	SPI-Flash Disable
JP3	0	SPI-Flash Enable
JP4	1	k8 power sequency function is Disable
JP4	0	k8 power sequency function is Enable
JP5	1	Disable WDT reset PWROK
JP5	0	Enable WDT reset PWROK
JP6	1	Parallel VID output
JP6	0	Serial VID output
JP7	1	Enable Dual BIOS Function
JP7	0	Disable Dual BIOS Function

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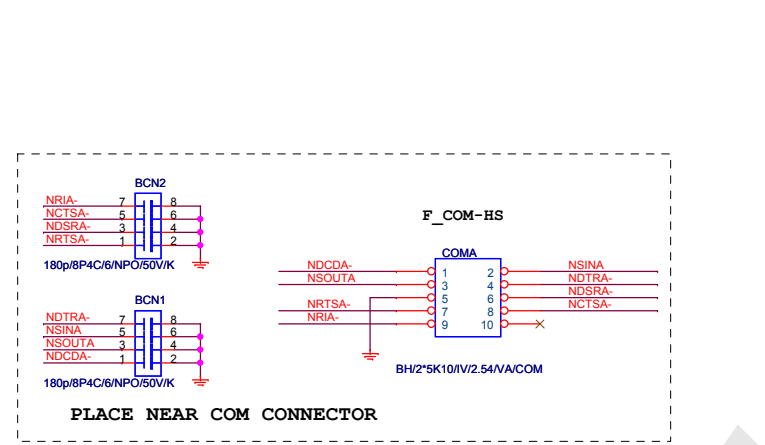
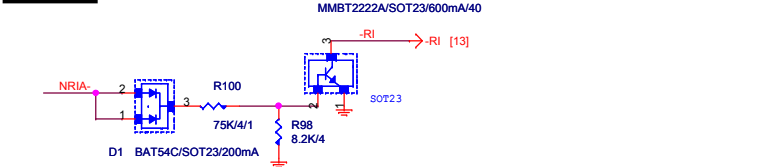
Title			ITE 8720 LPC IO
Size B	Document Number	GA-H55M-D2H	
Date:	Wednesday, June 30, 2010	Sheet	18 of 34



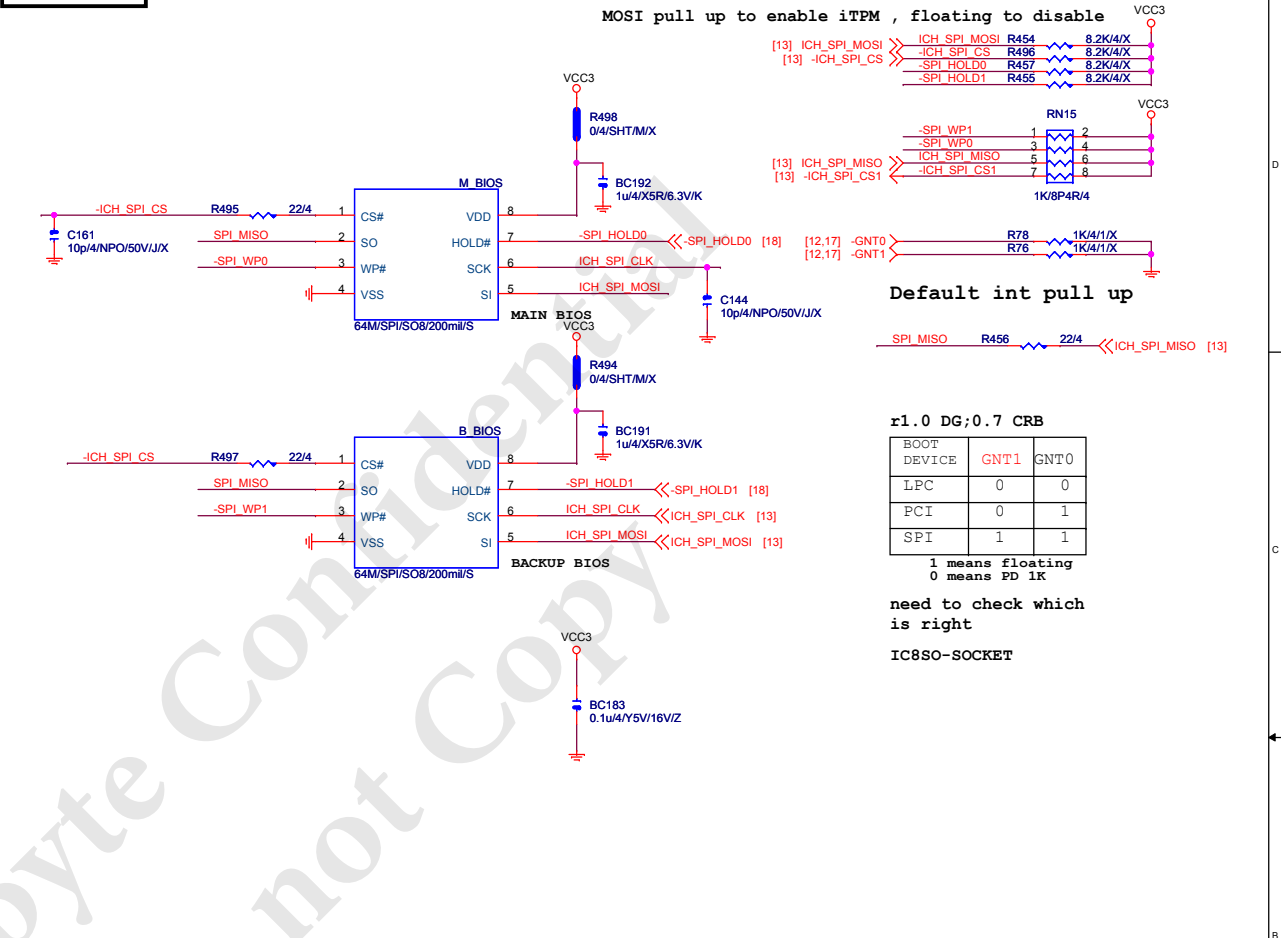
# COMB



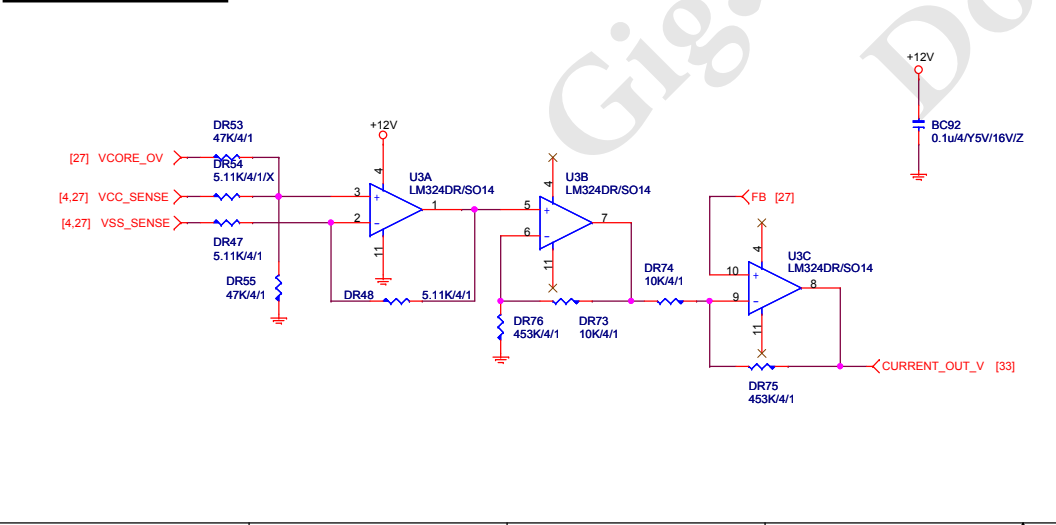
# RING IN



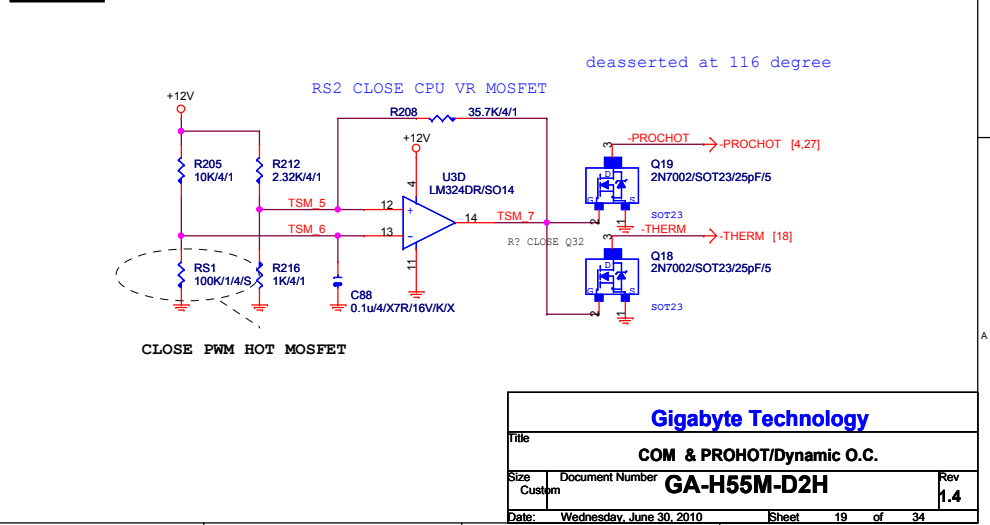
# DUAL BIOS



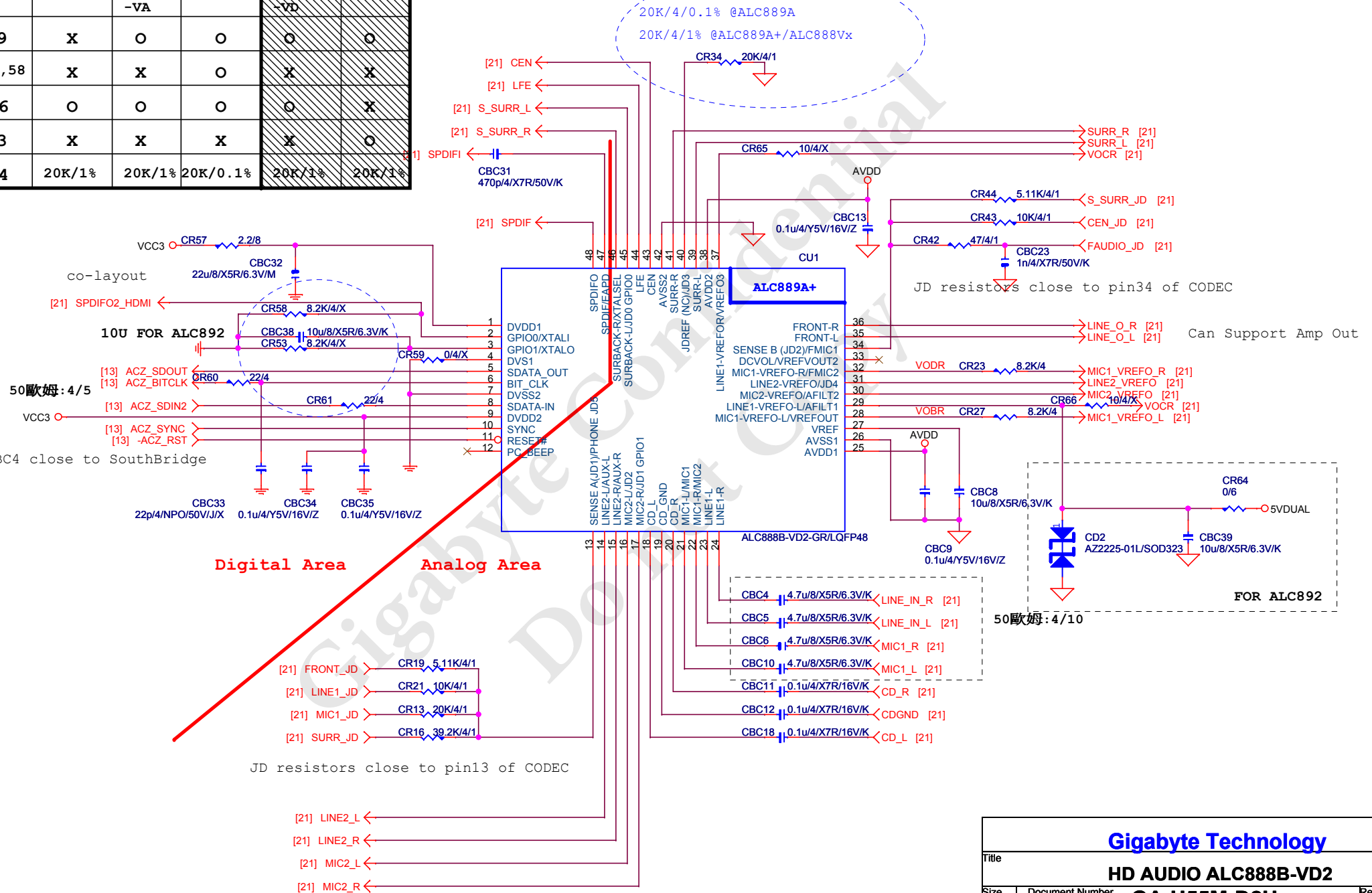
# DYNAMIC CURRENT OC



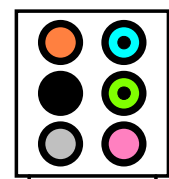
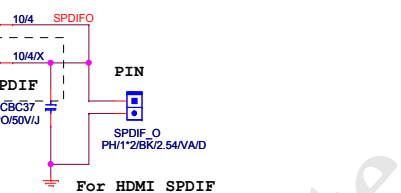
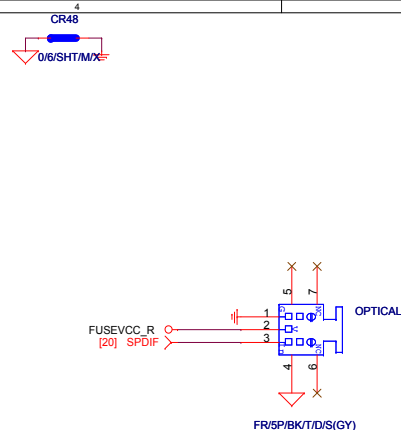
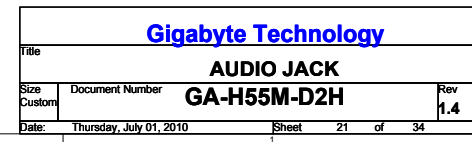
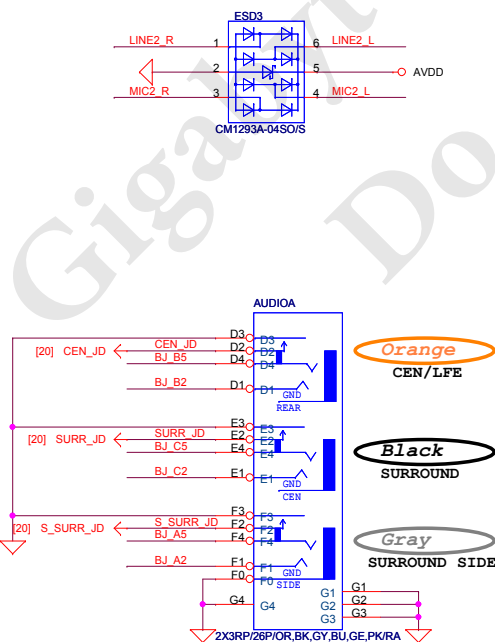
# -PROHOT



	ALC888B	ALC888 -VA	ALC889A	ALC888 -VD	ALC892
CR59	X	O	O	O	O
CR53,58	X	X	O	X	X
CR56	O	O	O	O	X
CR63	X	X	X	X	O
CR34	20K/1%	20K/1%	20K/0.1%	20K/1%	20K/1%

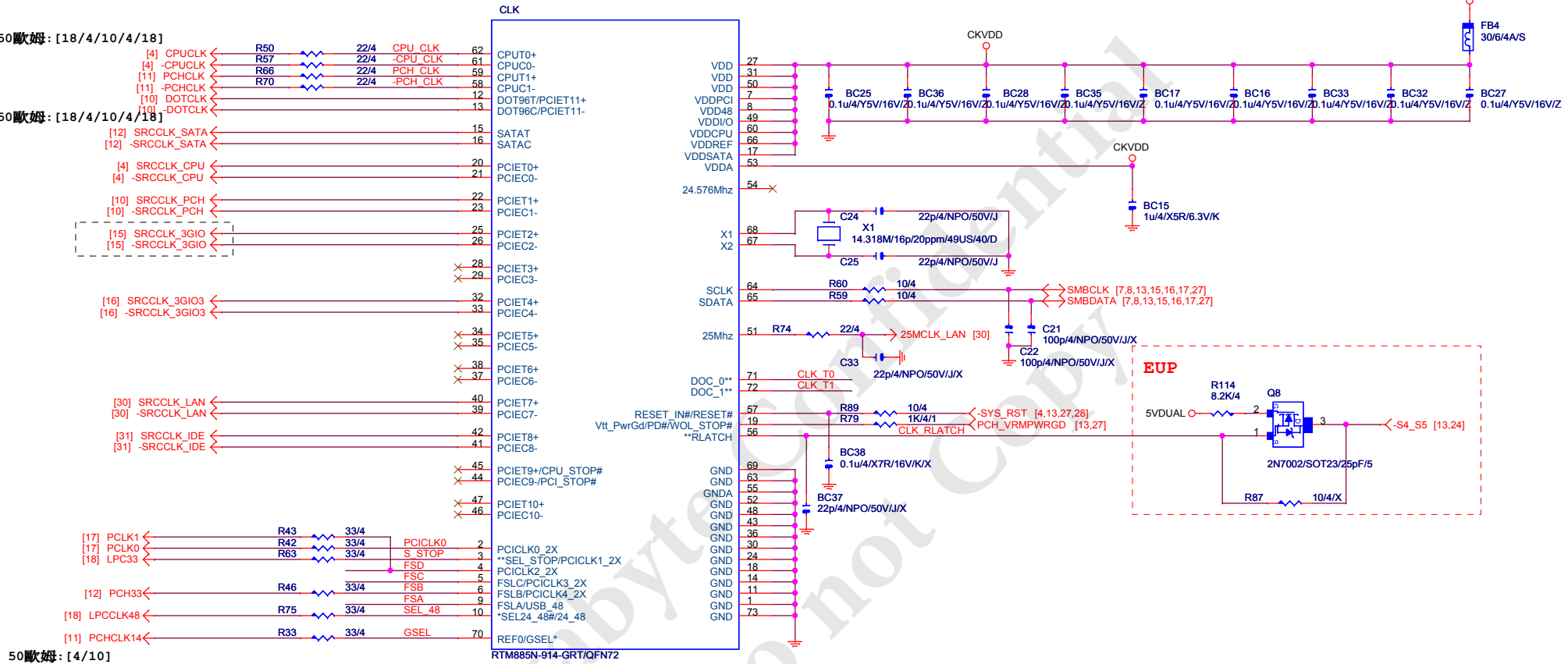


Can Support Amp Out

[illegible]

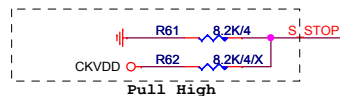
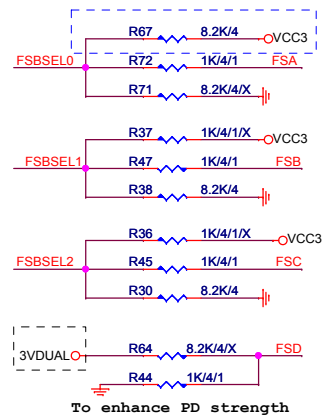
50歐姆:[18/4/10/4/18]

50歐姆:[18/4/10/4/18]



50歐姆:[4/10]

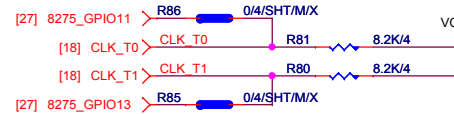
RTM885N-914-GRT/QFN72



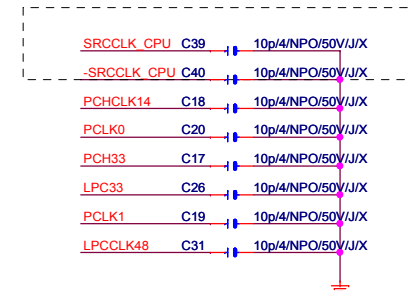
GSEL=1, 96Mhz from 12/13  
GSEL=0, 100Mhz from 12/13

SEL\_48=1, 24Mhz from pin10  
SEL\_48=0, 48Mhz from pin10

FSC	FSB	FSA	CPU
0	0	0	266MHz
0	0	1	133MHz
0	1	0	200MHz
0	1	1	166MHz
1	0	0	333MHz
1	1	0	400MHz



**SEL\_STOP:** latched input to select pin functionality  
1 = Selects pin 44/45 to be PCI\_STOP#/CPU\_STOP#  
0 = Selects pin 44/45 to be PCIE outputs ;  
3.3V PCICLK output

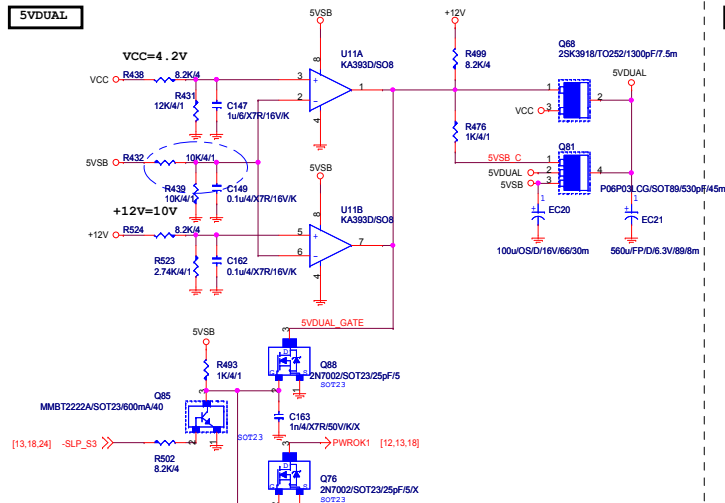


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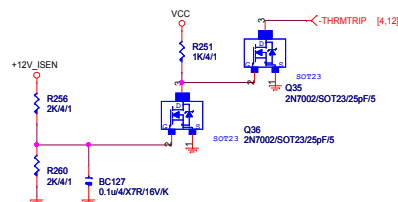
Title			CK505 CLK GEN
Size			GA-H55M-D2H
Date:			Wednesday, June 30, 2010
Sheet			22 of 34
Rev			1.4



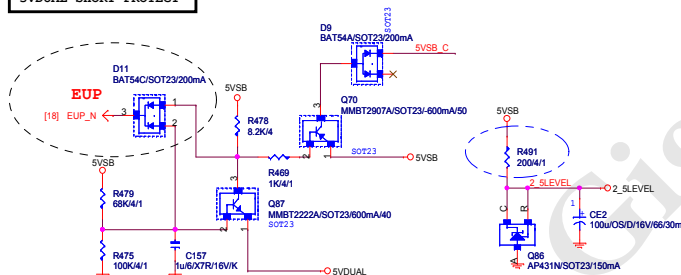
## 5VDUAL



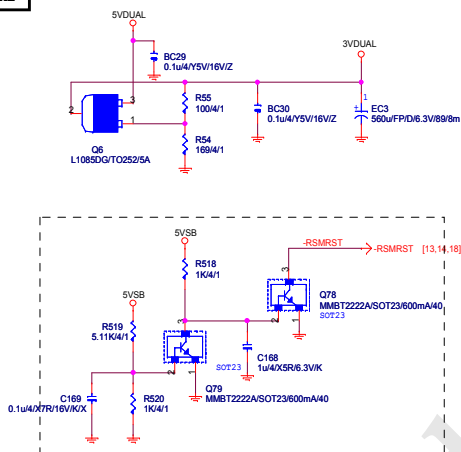
## +12V SHORT PROTECT



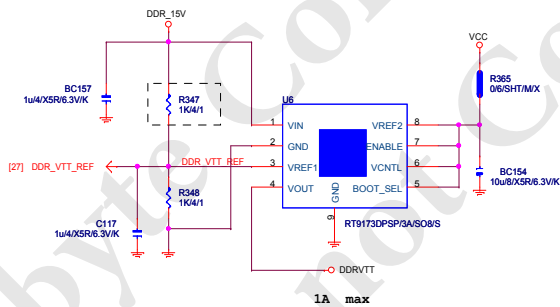
## 5VDUAL SHORT PROTECT



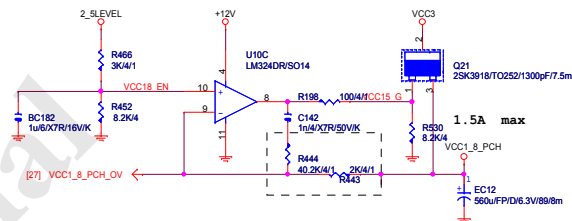
## 3VDUAL



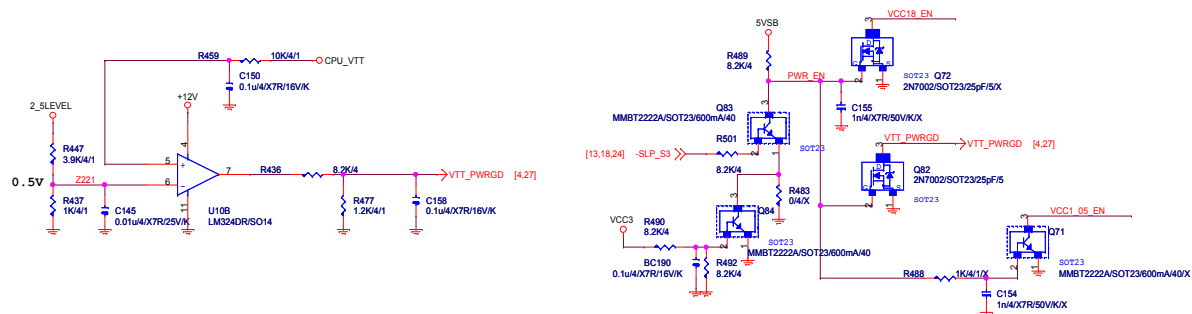
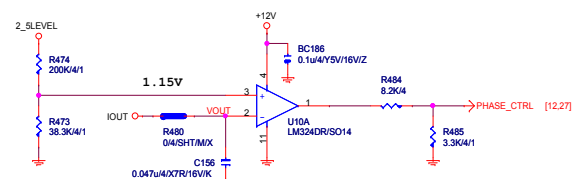
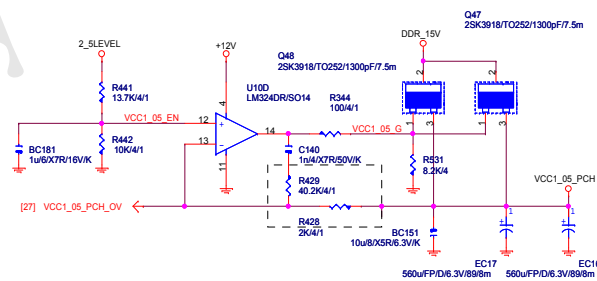
## DDRVTT



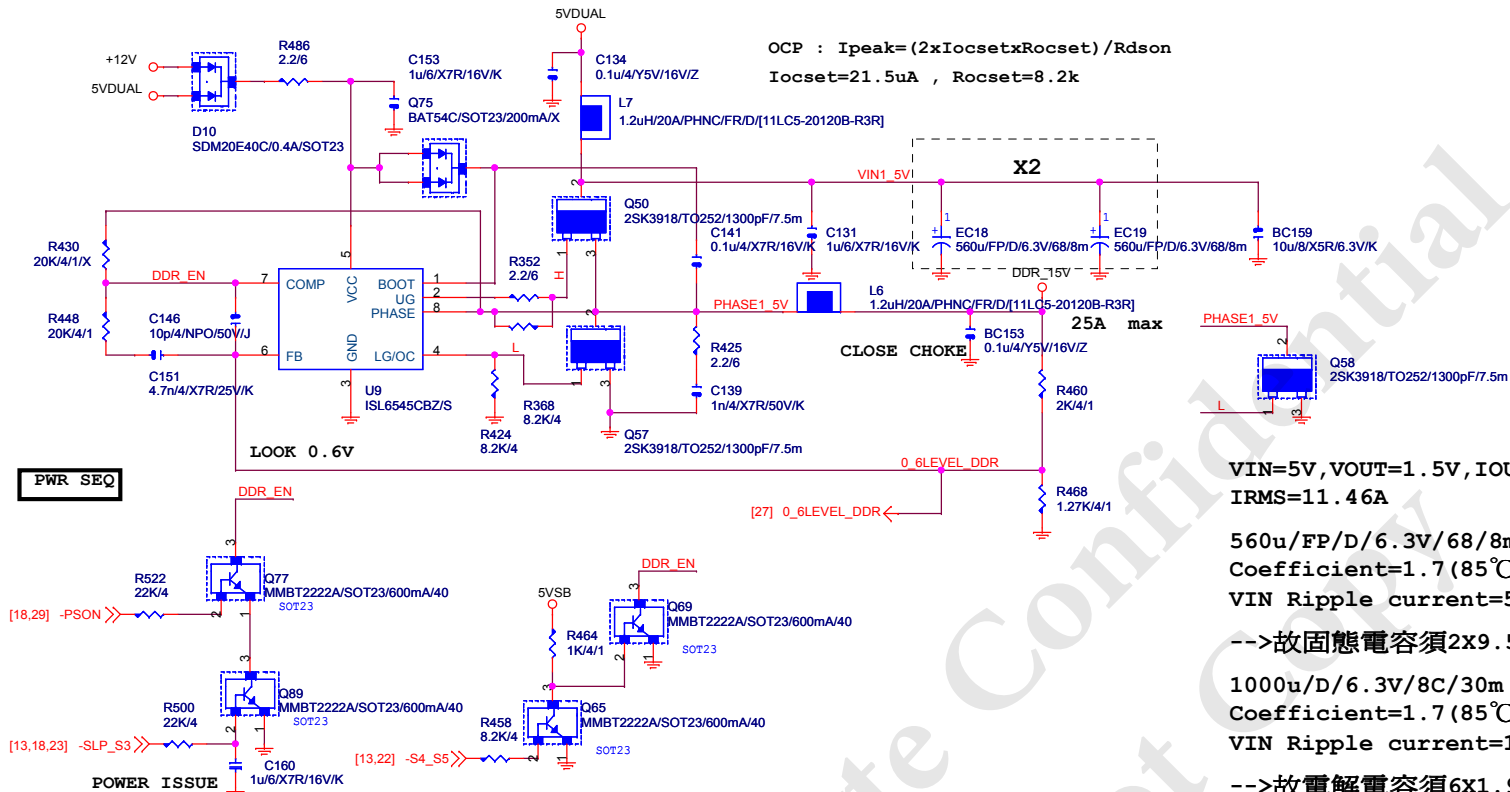
## VCC1\_8\_PCH



## VCC1\_05\_PCH



# DDR1\_5V



VIN=5V, VOUT=1.5V, IOUT=25A, PHASE=1

IRMS=11.46A

560u/FP/D/6.3V/68/8m RIPPLE CURRENT=5.6A

Coefficient=1.7 (85°C), 1 (105°C)

VIN Ripple current=5.6X1.7=9.52A (85°C)

-->故固態電容須2X9.52=19.04>11.46A

1000u/D/6.3V/8C/30m RIPPLE CURRENT=1.14A

Coefficient=1.7 (85°C), 1 (105°C)

VIN Ripple current=1.14X1.7=1.938A (85°C)

-->故電解電容須6X1.938=11.628>11.46A

VIN=3V, VOUT=1.05V, IOUT=7.5A, PHASE=1

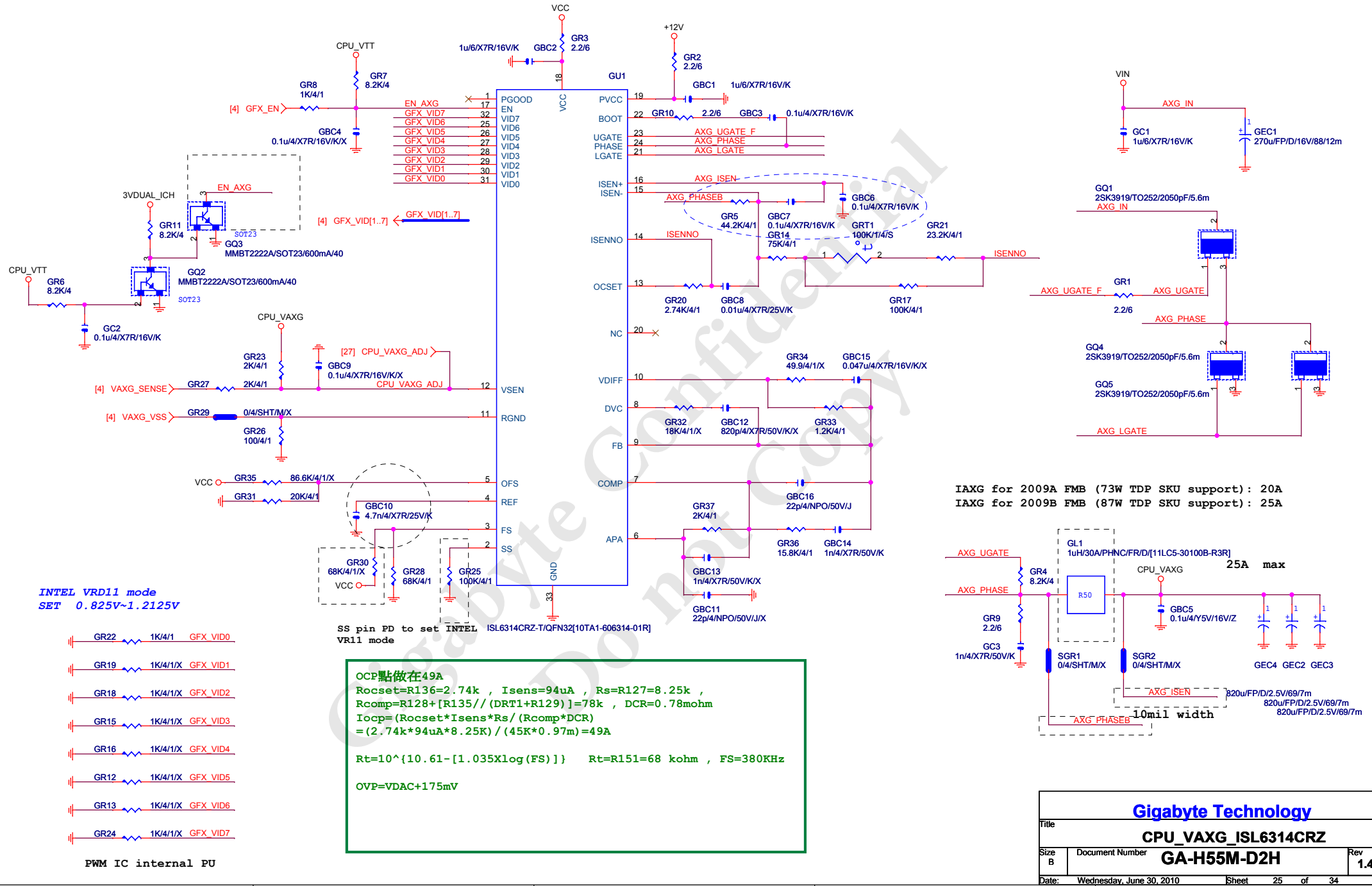
IRMS=3.5A

-->故固態電容須1X9.52=9.52>3.5A

-->故電解電容須2X1.938=3.876>3.5A

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Title		
DDR 15V		
Size	Document Number	Rev
Custom	GA-H55M-D2H	1.4
Date:	Wednesday, June 30, 2010	Sheet 24 of 34

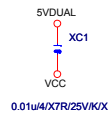
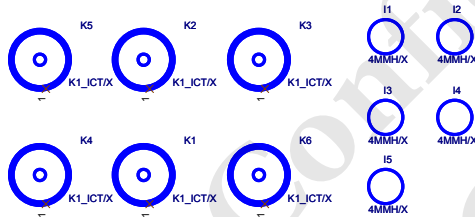
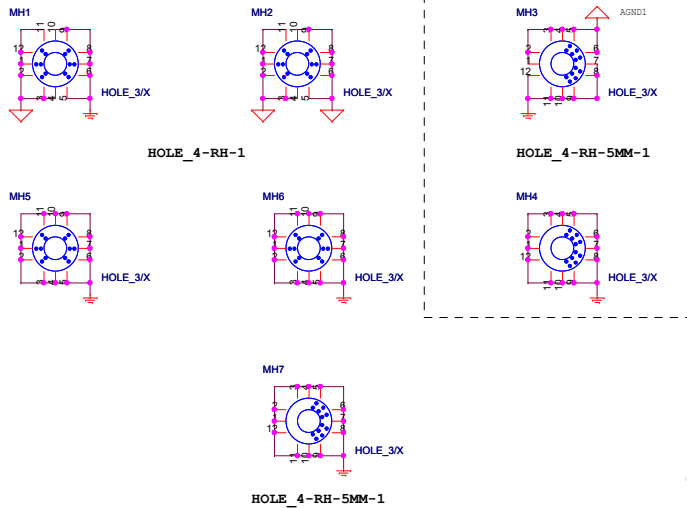
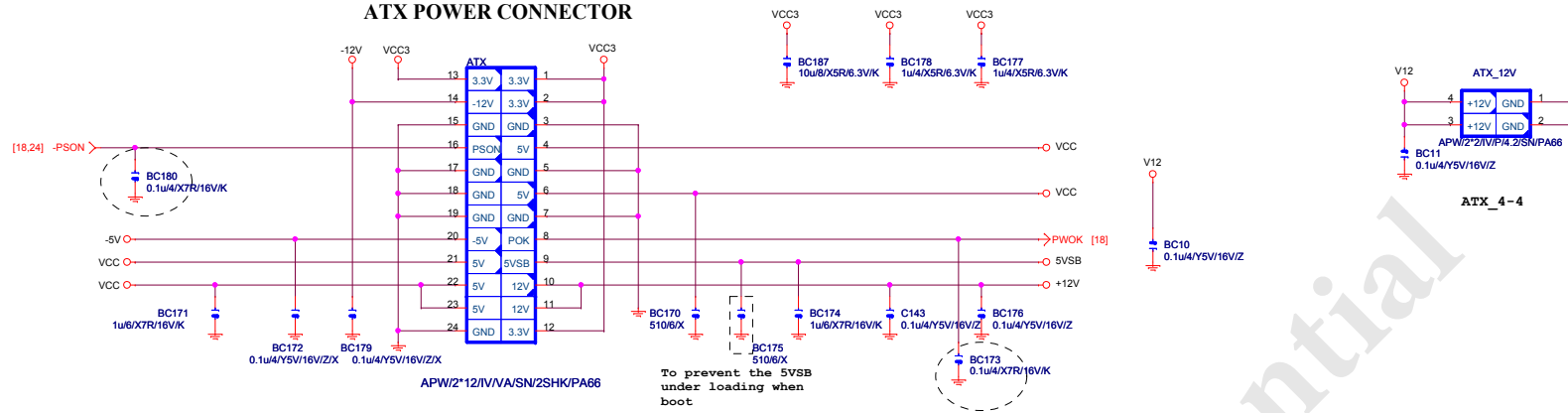






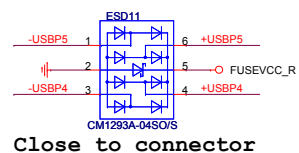
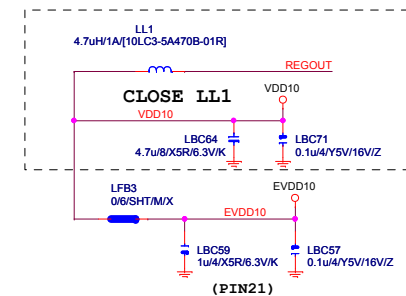
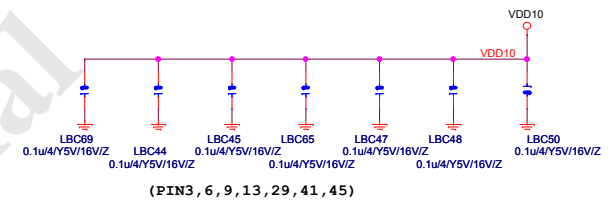
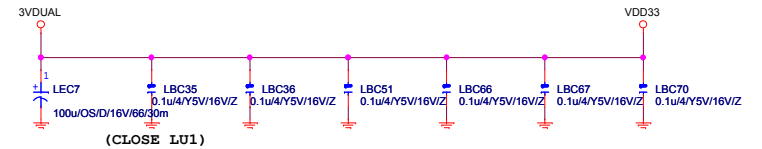
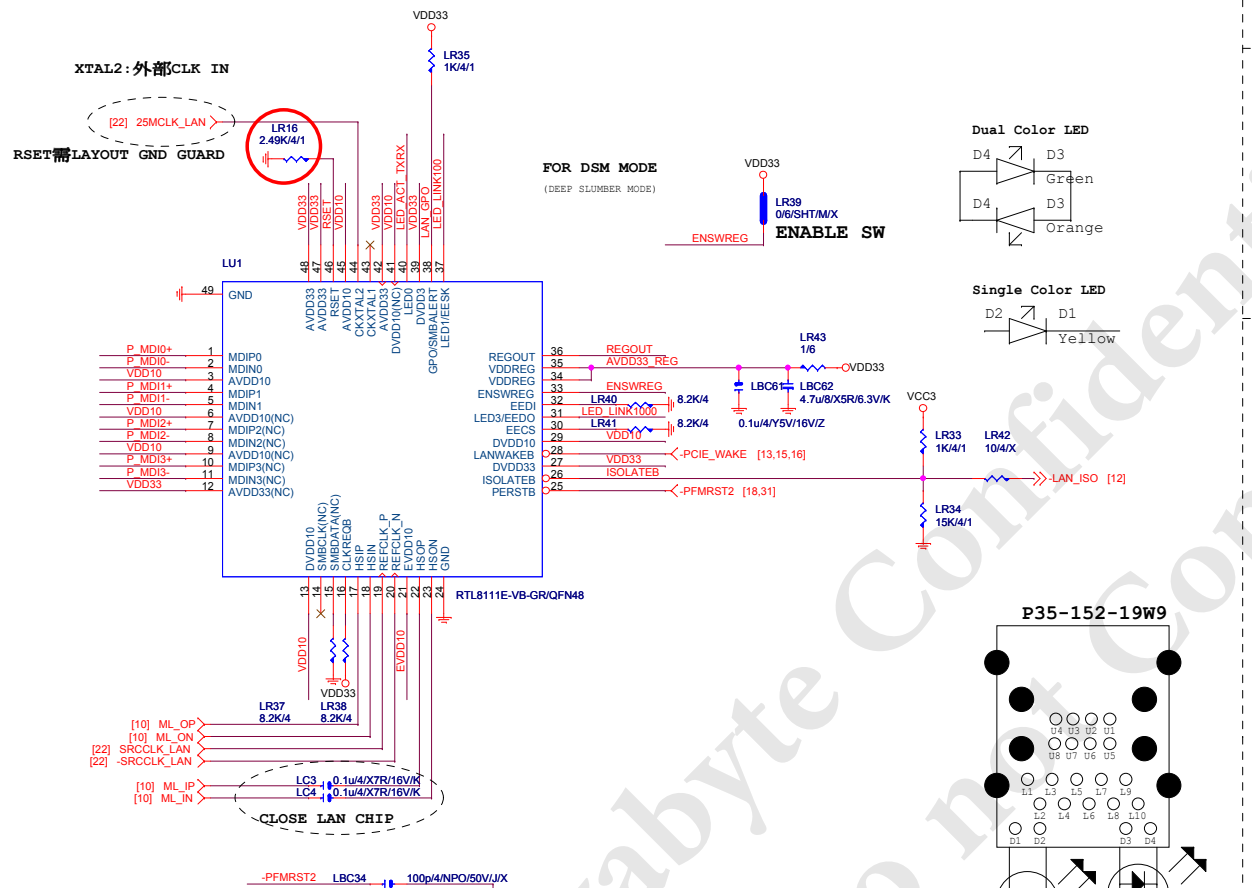


# ATX POWER CONNECTOR

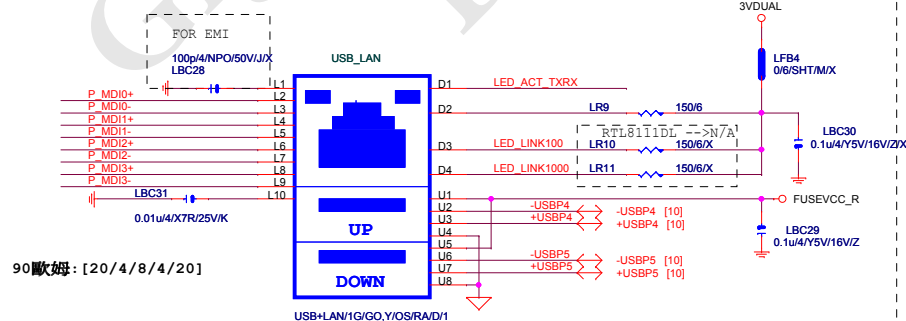




## PCIE-1G LAN

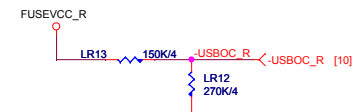
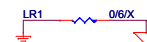


Close to connector

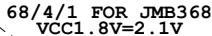


90歐姆: [20/4/8/4/20]

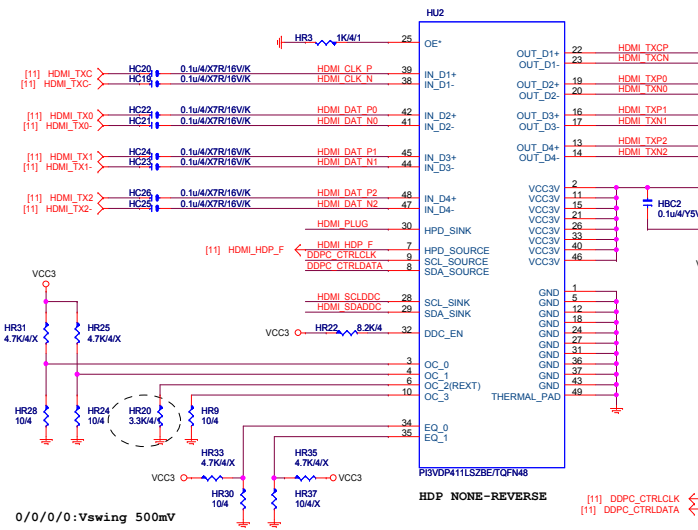
USB+LAN/1G/GO,Y/OS/RA/D/1



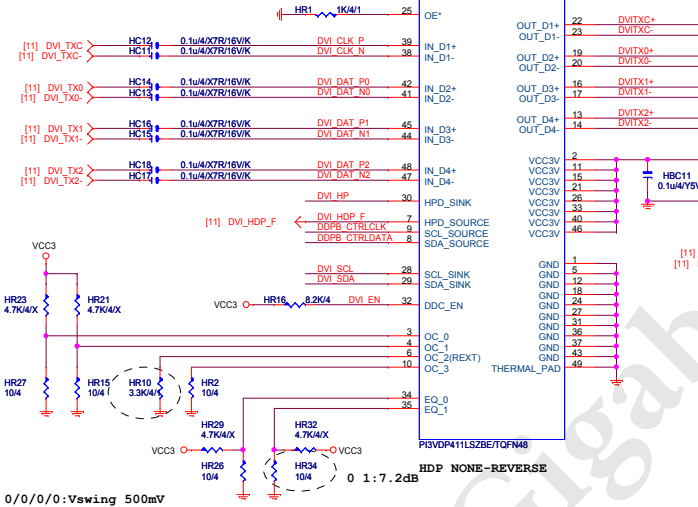
L1117LG/N/SOT223/1A

PH\_CBLID\_N PDIAGnA

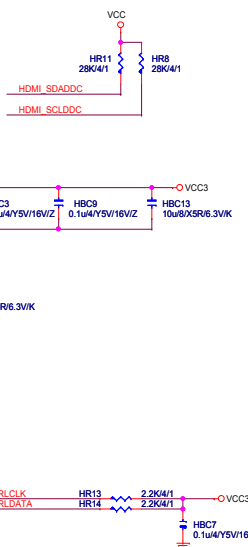
PH RESETnA	1	2	
PH_DD7	3		PH_DD8
PH_DD6	5		PH_DD9
PH_DD5	7		PH_DD10
PH_DD4	9		PH_DD11
PH_DD3	11		PH_DD12
PH_DD2	13		PH_DD13
PH_DD1	15		PH_DD14
PH_DD0	17		PH_DD15
	19		
PH_DMARQ	21	22	(#20 key-pin)
PH_DDIOW N	23	24	
PH_DIOR N	25	26	(#28 CSEL)
PH_IORDY	27	28	CSELA
PH_DMACK N	29	30	
PH_INTRQ	31	32	(#32 IOCS16)
PH_DA1	33	34	PH_CBLID N
PH_DA0	35	36	PH_DA2
PH_CS0 N	37	38	PH_CS1 N
DASPrxA	39	40	



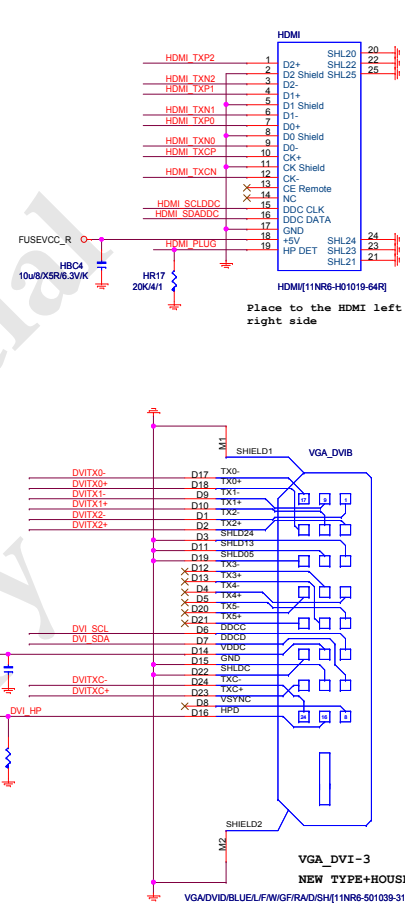
0 1:7.2dB



0 1:7.2dB

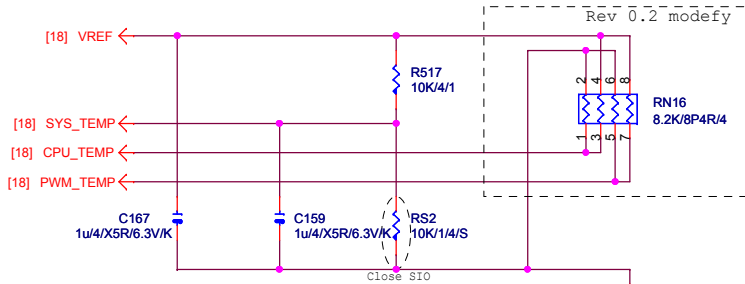


0 1:7.2dB

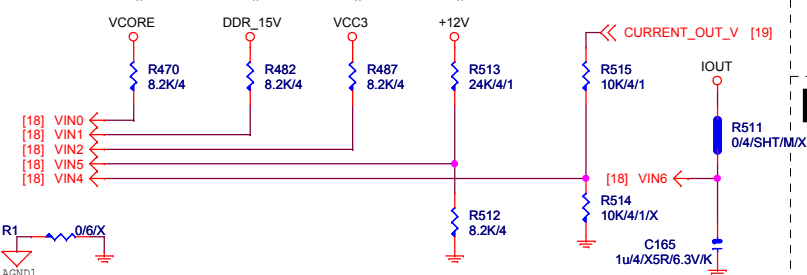


Place to the HDMI left & right side

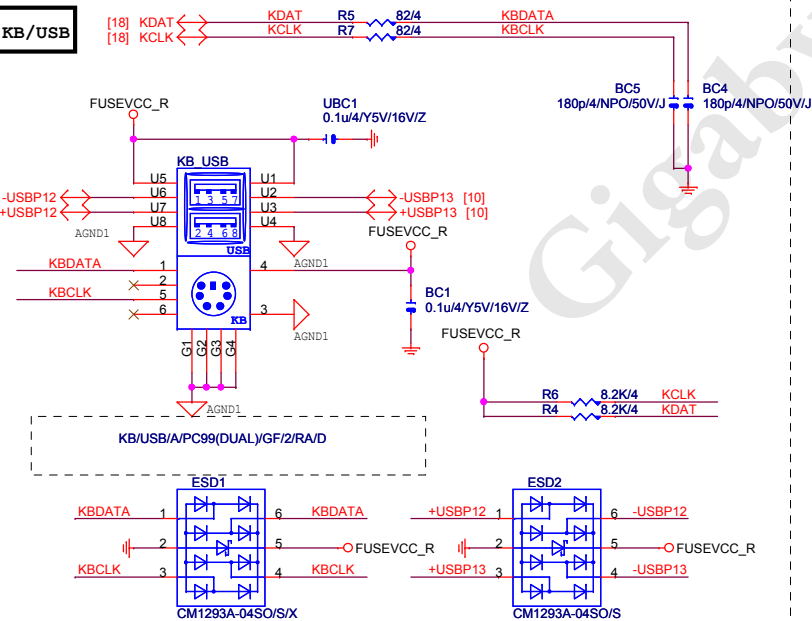
# TEMP H/W MONITOR



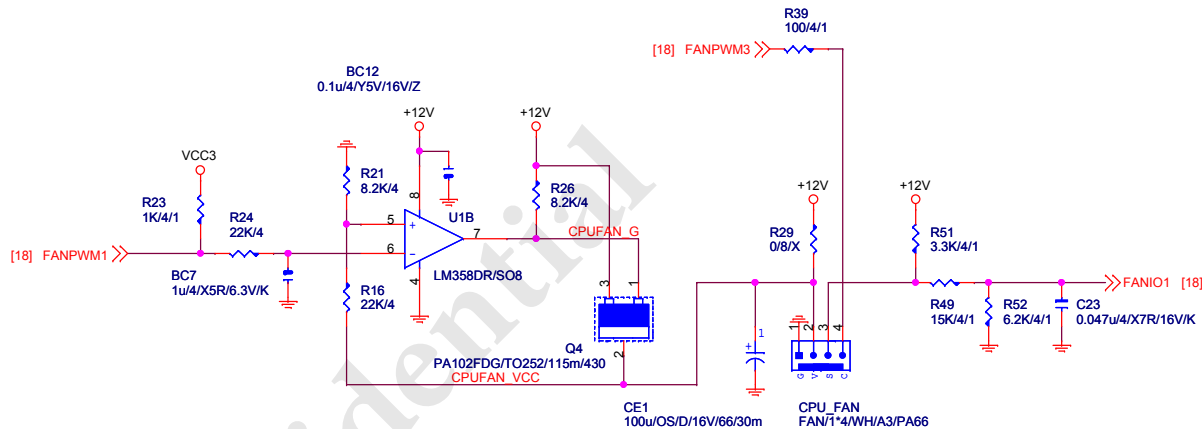
# VOLTAGE-- H/W MONITOR



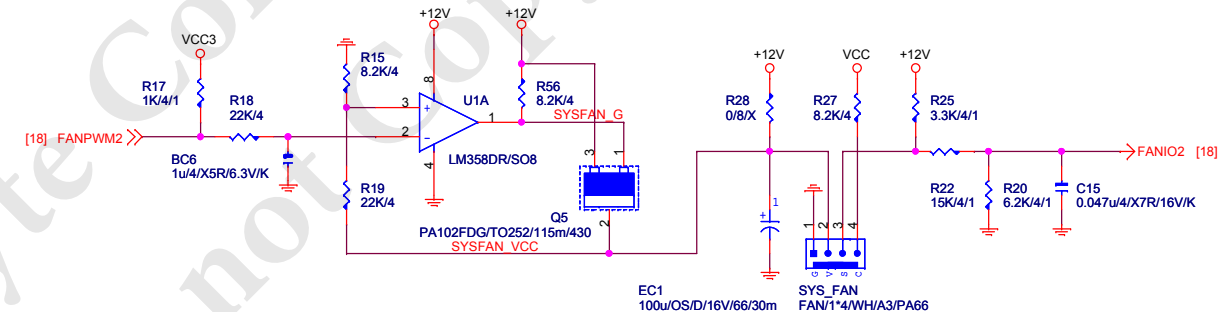
# KB/USB



# CPU SMART FAN



# SYS SMART FAN Linear SYS\_FAN



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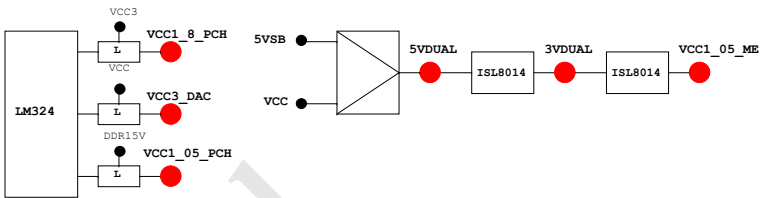
Title				Rev
HWM,KB/MS, FAN CTRL				
Size	Document Number			
Custom	GA-H55M-D2H			
Date: Thursday, July 01, 2010		Sheet	33	of 34

PCH GPIO LIST TABLE					
PIN NAME	PWR	AFTER PLT1ST	Default	USAGE	NOTE
GP0	MAIN	H-Z	GPI	-PECI_REQ	N/A
GP1/TACH1	MAIN		GPI	ICH_FAN_TACH1	N/A
GP2/PIRQE#	MAIN		GPI	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI	ICH_FAN_TACH2	N/A
GP7/TACH3	MAIN		GPI	ICH_FAN_TACH3	N/A
GP8	STBY	H	GPO	GPIO8	P/U 8.2K 3VDUAL
GP9/OC5#	STBY		NATIVE	OC5#	N/A
GP10/OC6#	STBY		NATIVE	OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE	-SMBALERT	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL
GP13	STBY	L	GPI	GPIO13	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE	OC7#	N/A
GP15	STBY	L	GPO	GPIO15	N/A
GP16	MAIN		GPI	-SKTOCC	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI	ICH_FAN_TACH0	N/A
GP18	MAIN		NATIVE	MB_ID0	P/D 8.2K GND
GP19	MAIN		GPI	-LAN1_ISO	P/U 8.2K VCC3
GP20	MAIN		NATIVE	LED_CTL	P/U 1K VCC3
GP21	MAIN		GPI	VCC18_PCH_OV2	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	VCORE_OV3	P/U 8.2K VCC3
GP23	MAIN		NATIVE	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	L	GPO	TLS	P/U 8.2K 3VDUAL
GP25	STBY		NATIVE	-CPU_STOP	P/U 8.2K 3VDUAL
GP26	STBY		NATIVE	-AC2_DET	P/U 8.2K 3VDUAL
GP27	STBY	H	GPO	GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO	GPIO28	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI	GPIO29	N/A
GP30	STBY	H-Z	GPI	S_PWR_ACK	P/U 100K 3VDUAL
GP31	STBY	H-Z	GPI	N/A(Reverse)	P/U 8.2K VCC3
GP32	MAIN	H	GPO	MB_ID1	P/D 8.2K GND
GP33	MAIN	H	GPO	LOAD-LINE	P/U 1K VCC3
GP34	MAIN	H-Z	GPI	-PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO	GPIO35	P/U 8.2K VCC3
GP36	MAIN		GPI	-LAN1_DSM	P/U 8.2K VCC3
GP37	MAIN		GPI	N/A	P/U 8.2K VCC3
GP38	MAIN	H-Z	GPI	VCORE_OV2	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI	-LAN_DSM	P/U 8.2K VCC3
GP40	STBY		NATIVE	OC1#	N/A
GP41	STBY		NATIVE	OC2#	N/A
GP42	STBY		NATIVE	OC3#	N/A
GP43	STBY		NATIVE	OC4#	N/A
GP44	STBY	L	NATIVE	N/A	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE	-LPCPME	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	PWR_LED	P/U 8.2K 3VDUAL
GP47	STBY		NATIVE	PSI_LED	P/U 8.2K 3VDUAL
GP48	MAIN	H-Z	IN	EN_PWM	P/U 8.2K VCC3
GP49	MAIN	H-Z	IN	VCC18_OV1	P/U 8.2K VCC3
GP50	MAIN		NATIVE	-REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	-GNT1	N/A
GP52	MAIN		NATIVE	-REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	-GNT2	N/A
GP54	MAIN		NATIVE	-REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	-GNT3	N/A
GP56	STBY		NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP57	STBY	H-Z	IN	VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE	F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE	-SUSTAT	N/A
GP62	STBY	L	NATIVE	SUSCLK	N/A
GP63	STBY	L	NATIVE	GPIO63	N/A
GP64	MAIN	L	NATIVE	CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE	CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE	CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE	CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE	VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY		NATIVE	1_05V_OV1	P/U 8.2K 3VDUAL
GP74	STBY	H-Z	NATIVE	1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL

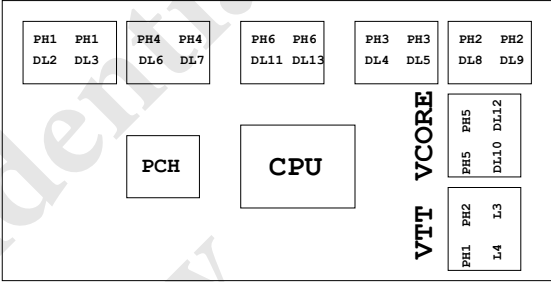
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRXL1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSIO	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VIDO5/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSB5W#/GP40	CSI_F0	BSEL166_1
SUSCH#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSSO1	MB_ID3	
PD7/GP77/BUSSO2	MB_ID4	
AFD#/GP86/SMB_C_R	32 PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VIDO1/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMB_C_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VIDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRX2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下:



BIOS超電壓對應表:

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

散熱模組料號:

8IBP:  
1.12SP2-01A001-Y1R/Y2R  
2.12SP2-01A001-Z1R/Z2R  
(HIBRID模組) 包材階

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH